DOST-ASTI Bids and Awards Committee
Invitation to Bid (Public Bidding)

ITB No:	19-07-2575	**Date:**	July-16-2019
PR No:	EPIIC P2-19-05-7828	**Date:**	May-29-2019
Source of Funds:			
Total ABC:	Php 3,007,000.00		
Time, Date & Venue of Pre-bid Conference:	July 25, 2019, 1:30 PM at DOST-ASTI		
Time and Date of Submission of Bids:	August 06, 2019, 12:00 PM		
Time, Date & Venue of Opening Bids:	August 06, 2019, 1:30 PM at DOST-ASTI		
Date of availability of Complete Set of Documents:	July 17, 2019		
Deadline of Potential Bidder's Clarifications:	July 27, 2019		
Deadline of ASTI's Supplemental Bid Bulletin:	July 30, 2019		
Delivery Schedule:			

The Advanced Science and Technology Institute (ASTI), through its Bids and Awards Committee (BAC), hereby invites all interested bidders to submit their bids for the item(s) listed below. Guidelines regarding the format, eligibility, technical and financial documents needed are described in the Instruction to Bidders of the Philippine Bidding Documents

Bidding will be conducted through open competitive bidding procedures using a non discretionary "pass/fail" criterion as specified in the 2016 R-IRR of RA 9184.

A complete set of Bidding Documents may be purchased by interested bidders upon payment of a fee for the Bidding Documents. It is also downloadable for free of charge at DOST-ASTI's website - ***www.asti.dost.gov.ph***

For further inquiries, contact ASTI's BAC Secretariat via email at ***bac-sec@asti.dost.gov.ph***. Interested bidders may also call the number - (632)-426-7423 and look for ASTI's BAC Secretariat.

Respectfully,

PEDRITO B. MANGAHAS
Chairperson, BAC-1

NO.	TECHNICAL SPECIFICATIONS	QTY	UNIT	UNIT PRICE(Php)	TOTAL PRICE(Php)
1	**Supply and Installation of Electronic Design Tools Software** *One (1) PCB Designer Software with the following specifications: I. Basic Specifications: 1. Supports workflow from placement and routing, all the way through to manufacturing 2. Supports design partitioning, RF design capabilities, and interconnect design planning 3. Certified for "Fit for Purpose - Tool Confidence Level 1 (TCL1)" thereby enabling the software to meet stringent ISO 26262 automotive safety requirements 4. 99 year license with one (1) year support and maintenance II. Features: 1. Design Authoring:	1	unit	3007000.00	3,007,000.00

1.a. Supports flat and hierarchical schematic creation
1.b. Page navigation, Management, Hierarchy Viewer
1.c. Variant Editor
1.d. Project Manager
1.e. Cross Referencer
1.f. Archiver
1.g. Design Differences
1.h. Properties Worksheet, Differential Pair Worksheet
1.i. Support for Net Classes
1.j. User Customization
1.k. Part Manager
1.l. Bill-of-Materials Generator
1.m. Physical Design Reuse, Hierarchical Block Reuse
1.n. Blocks and Sheets Importer
1.o. Copy Projects or Copy/Paste Within and Between Designs
1.p. Design Rules Checker
1.q. Verilog and VHDL Netlisting
1.r. Analog/Mixed Signal Integration
1.s. Physical Realization for mainstream FPGA's (from Xilinx, Actel, and Intel)
1.t. Customizable Menus and Commands using text-based scripting language.
1.u. Cross-Probing with PCB Editor
2. Design Entry:
2.a. Provides fast, intuitive schematic editing
2.b. Boosts schematic editing efficiency through design reuse
2.c. Automates the integration of field programmable gate arrays (FPGAs) and programmable logic devices (PLDs)
2.d. Makes changes quickly through a single spreadsheet editor
2.e. Imports and exports every commonly used design file format
2.f. Integrates with a robust Component Information System (CIS) to promote reuse of preferred, current parts
3. Constraint Manager
3.a. Supports to define, view and validate constraints at each step in the design flow, from design capture to floorplanning to design realization.
3.b. Constraint Manager for:
3.b.i. Physical, spacing, and same net rules
3.b.ii. Properties and DRCs
3.b.iii. Differential pair rules
3.b.iv. Region rules
4. Have floorplanning, placement, placement replication capabilities
5. Supports Design for Assembly (DFA) functionality, Design for Fabrication (DFF) functionality, Design for Testing (DFT) functionality
6. Dynamic feedback on DFA compliance during placement
7. Import/Export of IDF3.0 and DXF file format
8. EDMD schema-based ECAD-MCAD co-design
8.a. Efficient, Incremental Collaboration with IDX
8.b. 3D Visualization with STEP
9. Native 3D Viewer

9.a. 3D interference checking with clash markers
9.b. 2D and 3D view cross probing to enable quick updates based on issues or changes discovered when viewing in 3D
10. Hierarchical interconnect flow planning
11. Length-based rules for high-speed signals
12. Constraint-driven flow for length-based high-speed signals
13. Match groups, layer sets, extended nets
14. T-point rules (pin to T-point)
15. 6-layer automatic shape-based autorouter
16. High-speed rules-based autorouting
17. Layer-specific rules-based autorouting

III. This Software should be capable of the following upgrades should the End-user decide to procure any in the future:
1. Design planning - plan spatial feasibility analysis and feedback
2. Design planning - generate topological plan
3. Design planning - Convert topological plan to traces
4. Electrical Constraints Sets (high speed)
5. Physical, Spacing Constraints (high speed)
6. Same Net Spacing (high speed)
7. High-Speed Model Assignment (high speed)
8. HS Signal Topology Editor (high speed)
9. Component Revision Manager (high speed)
10. Auto-interactive Delay Tuning (high speed)
11. Constraint Manager: Electrical rule set (relection, timing, crosstalk) (high speed)
12. Constraint-driven flow using electrical rules (high speed)
13. Electrical constraint rule set (ECSets) / topology apply (high speed)
14. Formula and relationship-based (advanced) constraints (high speed)
15. Backdrilling (high speed)
16. Die-to-die pin delay, dynamic phase control, Z-axis delay (high speed)
17. Return path management for critical signals (high speed)
18. Constraint Manager: HDI rule set (miniaturization)
19. Micro-via and associated spacing, stacking, and via-in-pad rules (miniaturization)
20. Constraint-driven HDI design flow (miniaturization)
21. Manufacturing rule support for embedding components (miniaturization)
22. Embedded components on inner layers (miniaturization)
23. HDI micro-via stack editing (miniaturization)
24. Dynamic shape-based filleting, line fattening, and trace filleting (miniaturization)
25. Hug contour routing (Flex) (miniaturization)
26. Support for cavities on inner layers (miniaturization)
27. Manage Shared Area (team)
28. Assign, Notify Teams (team)
29. Dashboard View of Blocks in the Project (team)
30. Merge / Split Blocks (team)
31. Locking Team (team)
32. Out-of-Date Check (team)

	33. Concurrent team design - layer-by-layer partitioning (team) 34. Concurrent team design - functional block partitioning (team) 35. Concurrent team design - team design dashboard (team) 36. Concurrent team design - soft nets (team) 37. Edit constraints in a partition (team) 38. Manage net classes in a partition (team) 39. Parameterized RF etch elements editing (analog/rf) 40. Asymmetrical clearances (analog/rf) 41. Bi-directional interface with Keysight ADS (analog/rf) 42. Import Keysight ADS schematics into DE-HDL (analog/rf) 43. Layout-driven RF design creation (analog/rf) 44. Flexible Shape Editor (analog/rf) 45. 256-layer autorouting 46. DFM rules-based autorouting 47. Automatic trace spreading 48. ATP generation 49. Layer-specific rules-based autorouting 50. Table / Spreadsheet-Based Design Creation (Multi-Style) 51. Design Authoring Schematic Block Reuse (Multi-Style) 52. Import Verilog Netlist from Existing Design (Multi-Style) 53. Quick Connectivity Creation Functions (Multi-Style) 54. Import Connectivity using Text Format (Multi-Style) 55. Online Packaging (Multi-Style) 56. Associated Components (Multi-Style) 57. Schematic Generation for (Multi-Style) Designs (Multi-Style) 58. Import Verilog (Multi-Style) 59. Custom Reports (Multi-Style) 60. TCL Support for Scripting and Extensions (Multi-Style) 61. Route-Aware Automatic FPGA Pin Assignment (FPGA System Planner) 62. Automatic Symbol, Schematic Creation for FPGA Sub-System (FPGA System Planner) 63. Custom-Board ASIC Prototyping with FPGAs 64. Create and Publish Intelligent PDFs IV. Post-Qualification 1. External Providers shall provide a thirty (30) day trial version of the complete software that will be used by the End User for the Post-Qualification. The trial version shall be the exact same copy of the actual software that will be delivered. *Note: The External Provider shall provide their catalog of existing upgrades that complies with the above list. All inclusive of government fees, taxes and duties Delivery Date: 30 days upon issuance of NTP Delivery to: EPDC Building, MIRDC Compound, Gen. Santos Ave., Bicutan, Taguig City, Philippines				

TOTAL APPROVED BUDGET FOR THE CONTRACT (ABC):	Php 3,007,000.00

RESERVATION CLAUSE

The Advanced Science and Technology Institute reserves the right to accept or reject any proposal, to annul the bidding process, and to reject all proposals at any time prior to contract award, without thereby incurring any liability to the affected proponent or proponents.